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Remarks

Claims 1-15 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated October 20, 2006 indicated an objection to the drawings under 37 C.F.R. § 1.83(b), and the following: claims 1-15 stand rejected under 35 U.S.C. § 102(b) over Cassetti *et al.* (U.S. 6,311,302).

Regarding the objection to the drawings, per a telephone conversation with the Examiner on January 9, 2006, Applicant has amended figures 1 and 6. These amendments are fully supported by Applicant's specification (*see, e.g.,* paragraphs 0027 and 0028 for Fig. 1; and paragraph 0036 for Fig. 6). Applicant notes that the amendments to figures 1 and 6 correspond to figures 1 and 6 of U.S. Provisional Patent Application Number 60/435,395, to which the instant application claims priority. Therefore, Applicant requests that the objection to the drawings be removed.

Applicant respectfully traverses the Section 102(b) rejections of claims 1-15 because Office Action fails to cite prior art that corresponds to all of the claimed limitations, including those directed to the setting and storage of bits in a test access port (TAP) controller. For instance, regarding independent claim 1, the Office Action fails to cite to any portion of the Cassetti reference that corresponds to claimed limitations directed to resetting a first bit to a known state in each of a plurality of TAP controllers. The cited portions of Cassetti concern the storage of instructions in an internal test link module (TLM) that is separate from TAP controllers, thus failing to correspond to claimed limitations directed to TAP controller-based instruction storage. For example, FIG. 1 of the Cassetti reference shows a multi-core IC with the cores having multiple TAP controllers (TLM core 1 with TAP controllers 16 and 18) and an internal TLM including a TLM register (20) that stores a decodable instruction and a cell (22) for a supplemental extension bit (*see, e.g.,* col. 3:20-37 and col. 4:41-45). As such, Applicant submits that these cited portions of the Cassetti reference fail to correspond to claimed limitations directed to resetting a first bit in each of a plurality of TAP controllers to a known state and further producing a first signal based at least in part on the state of the

first bits. Accordingly, the Section 102(b) rejections of claim 1, and claims 2-11 that depend from claim 1, are improper and Applicant requests that they be withdrawn.

Regarding independent claim 12, the Office Action fails to cite to any portion of the Cassetti reference that corresponds to claimed limitations directed to each of the plurality of TAP controllers having at least one switch bit and the routing logic selectively connecting to one of the plurality of TAP controllers based at least in part on the state of the switch bits. As discussed above, the cited portions of Cassetti concern storing instructions in an internal TLM that is separate from the TAP controllers (*see, e.g.*, Fig. 1; col. 3, lines 20-37; col. 4, lines 41-45). As such, Applicant submits that the Office Action fails to cite to any portion of the Cassetti reference that corresponds to the routing logic selectively connecting to one of the plurality of TAP controllers based at least in part on the state of the switch bits as claimed in claim 12. Therefore, the Section 102(b) rejections of claim 12, and claims 13-15 that depend from claim 12, are improper and Applicant requests that they be withdrawn.

Applicant notes that minor amendments have been made to claim 1 to facilitate consistency among dependent claims and remove example reference numbers (*e.g.*, in dependent claims referring back to "step" type limitations), to claim 4 to remove an example reference number and to claim 12 for readability. These amendments are not made to overcome any issues relating to patentability or to overcome the rejections raised by the Office Action, which should be removed for the reasons discussed above.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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